P-55: A 10-bit Digital-to-Analog Converter using Active Resistor Strings for TFT LCDs

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Abstract

A general source driver IC used in TFT (Thin Film Transistor) LCD (Liquid Crystal Display) is non-linear passive resistor string DAC (Digital to Analog Converter) architecture. However, It has the limits for satisfaction needs of market. In this paper, a new linear active resistor string DAC architecture of the source drive IC used in the TFT LCD is proposed. A new linear active resistor string DAC architecture is capable to support more size efficiency and multiple gamma value and reduction RC delay. It is implemented in 0.35μ m CMOS process, and INL & DNL of active resistor string DAC are ±0.5 LSB and ±0.3 LSB each other

1. Introduction

TFT LCD is the most popular display device nowadays. The range of usage is widening from monitor to large TV. In case of large TV, high resolution, high color depth and high speed operation such as 120Hz are required for high display quality. So, TFT LCD source driver IC also requires multi gamma function, 10bit color, and high speed operation. These needs are difficult to be met because they conflict with the basic virtue of TFT LCD source driver IC, small size for low cost, channel output accuracy and low power consumption.

In this paper, a linear active resistor string DAC would be proposed for resolve the problem. It supports multi gamma function. More over, it is more advantageous in RC delay and more size efficiency than passive resistor string DAC.

2. Prior art of TFT-LCD source driver IC

A conventional 10bit LCD driver IC realized by using 10bit non linear DAC. In this case, 1024 resistor string with different values and 10bit decoder with MOS switches are required Though, resistor string is difficult to match different resistor values in the layout process, it can be a ideal voltage source. It has advantage of channel output accuracy because there is one reasonably ideal voltage source inside IC. However, when 10 bit IC is implemented, the size of decoder of 1 channel becomes as 4 times as existing 8 bit, because increasing 1 bit makes the size of decoder of 1 channel twice. In addition, when 10 bit IC is implemented, decoder stage becomes gaining 2 stages more than 8 bit, because increment of 1 bit makes 1 more decoder stage. Consequently, RC delay makes problems and it runs counter to high speed operation

2. A linear active resistor string DAC

2.1 A linear active resistor string DAC

Figure 1 shows a active resistor string DAC. The most important basic concept is that MOS transistor connected in series is used as resistor string. Active resistor string DAC utilizes linear gamma correction. In this case, the resistors with same values are used in linear gamma correction. If MOS transistors used in resistor string have all the same Rds, it can absolutely substitute for passive resistor string. In resistor string, regular quantity of current, about 400μ A, should flow. It is important in terms of influence on electric current consumption of LCD panel and RC delay of decoder. MOS transistor used as active resistor runs in the linear area by the reason that Vds is approximately 7.5/4096=2mV. MOS transistor in the linear area is able to generate the target figure of resistance more easily and accurately rather than passive resistor.

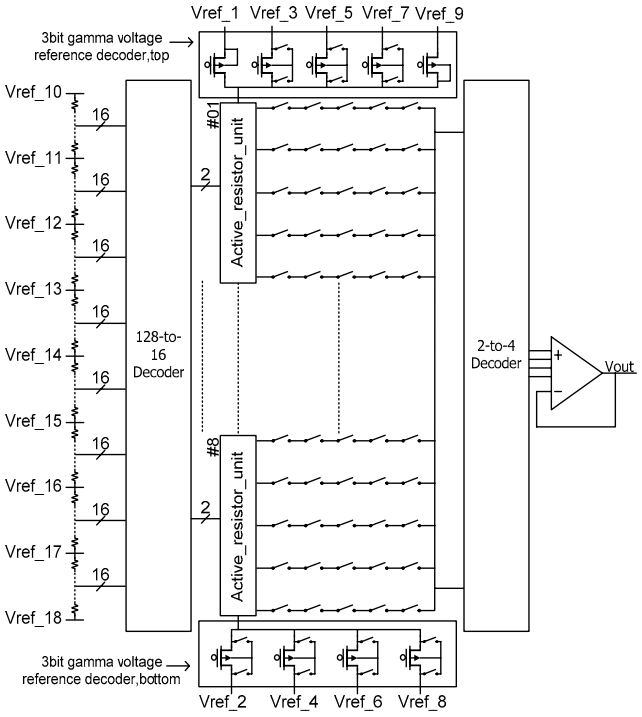

Fig 1. A 10bit linear active resistor string DAC with an interpolating buffer AMP

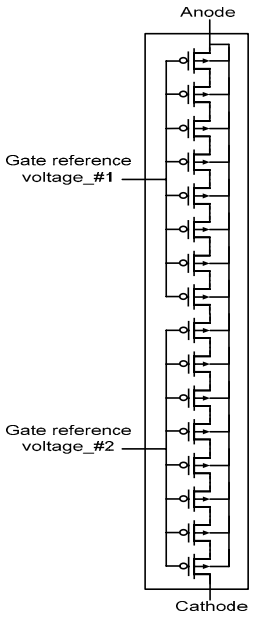

Fig 2. Active resistor unit

Moreover, the value of resistor is possible to be changed by adjusting Vgs. That can be implemented as active voltage reference which is able to control the value of electrical current flowing in resistor variably.

$$I_{D,lin} = \mu_p C_{ox} \frac{W}{L}[(Vgs - Vth)Vds - \frac{1}{2}Vds^2]$$

In order to have same Rds, widths, lengths, Vgs, Vds, Vth of every MOS Transistor should be also same. It is possible to adjust width, length which are decided by circuit designer. If MOS Transistor string which components have same value of W, L, Vgs, Vth is put between gamma voltage references which are arranged to regular gap as each one's, every transistor has same Vds. And body effect should be removed for making Vth same. The problem of body effect could be solved by separating bulk of MOS Transistor and connecting it with source. The values of voltage in linear gamma correction are symmetrical vertically with respect to line of VDD/2 value. For example, as Vref_1 is equal to voltage of MOS Transistor's source, Vref_10 becomes equal to one of gate. And, in case of Vref 2, Vref_11 also becomes same as one of gate. As using above two statements, it should be noted that Vref_1-Vref_10 = Vref_2 – Vref_11. Therefore, Vgs of all transistor can be kept constantly.

2.2 Implementation

Figure 1 is a real implemental drawing. As referenced above, we adapted linear gamma system, because it is more suitable for maintaining Rds of MOS Transistor regularly. In order to implement of 10 bit non linear, 12 bit linear gamma correction is generally used. But 10 bit gamma correction is used, because application environment has supported 10 bit system. Moreover, semi-conductor manufacturing process doesn't support isolation of Pwell , so bulk of NMOS can not be separated. For these reasons, upper VDD/2 range using PMOS except subordinate range of VDD/2 was only implemented.

3 bit gamma voltage reference decoder of figure 1 switches Vref_1 to Vref_9 to source and drain of active resistor unit string.

Active resistor unit shown by Figure 2 is a series connection of 16 PMOS transistors, and linear active resistor DAC has 8 active resistor units, as shown at Figure 1, so it is included that there are totally 128 series connections of PMOS transistor ($8 \times 16 = 2^7 = 128$).

The anode and cathode of each active resistor units are switched to voltage reference from Vref_1 to Vref_2 in order, which means that $2^3 \times 2^7 = 2^{10} = 1024$, thus this system has the same effect like 1024 resistors. That is, 2^{10} voltage levels can be made with 2^3 gamma reference voltages switching and 2^7 PMOS transistor strings. And 12 bit voltage levels can be made using 2 bit interpolating buffer Amp. However, only $32(=2^5)$ voltage levels out of the $128(=2^7)$ voltage levels which were made of active resistor unit are used, because application environment has supported 10 bit. Therefore, 10 bit(=1024) voltage levels are made using 5 bit decoder between active resistor unit and 2 bit interpolation buffer.

In the Fig. 1, 3 bit gamma voltage reference decoder is composed of PMOS transistor which contains switch at the bulk node because of preventing from reverse bias between source and bulk of PMOS transistor. The bulk's voltage of PMOS Transistor should be always higher than that of source and drain. If 0.7V of voltage is biased reversely, avalanche break down will be taken place, so current will be overflowed. For example, Vref_1 is connected to the source of active resistor unit, and Vref_2 does to the drain, the bulk switches of top 3bit gamma voltage reference decoder are all connected to Vref_1, the highest voltage. On the contrary, the bulk switches of bottom 3bit gamma voltage reference decoder prevent reverse bias, connected to opposite direction of Vref_2, the lowest voltage

As shown at Fig. 2, active resistor unit is composed of 16 PMOS transistor of which bulks are all connected and gates are connected with every 8 PMOS transistor. Ideally, in every PMOS transistor bulk and gate should be isolated each other. However, if so, lots of dimensions are needed, and we should find out proper midpoint between dimension and Output voltage error.

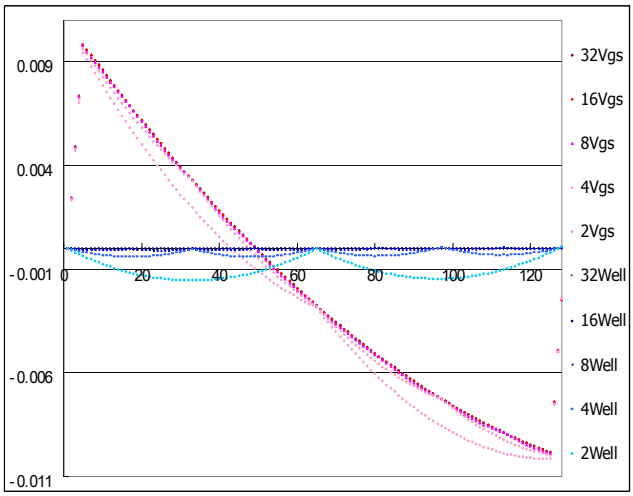

Fig 3. Output voltage error of 7bit active resistor string.

The graph of Fig. 3 shows Output voltage error of 7 bit PMOS transistor string. Red line graph shows Output voltage error that means every bulk of 128 PMOS transistors is common and gates are divided into 4,8,16,32 and 64 elements. In this case, Output voltage error of maximum ± 10mV occurs without reference to

the number of isolated gate. As the value of VDD is 15V, 1 step of Output voltage is equal to 7.5/4096=2mV. Output voltage error with isolating Vgs except isolating bulk can not be acceptable, so it is necessary to isolating bulks. On the contrary, blue line graph shows the Output voltage error that means every gate of 128 PMOS transistor is isolated and bulks are divided into 16, 32, and 64 elements respectively. In this case, max error is about 2mV. And in the case of dividing 128 PMOS into 4 groups, Output voltage error is able to be acceptable, because it is smaller than 1mV(=0.5 LSB). Actually in real implementation, we divided 128 PMOS bulks into 8 groups and gate into 16 groups. In other words, 16 of PMOS use bulk in common, and 8 of PMOS also use gate in common. Then, output voltage error is expected to be less than 0.1 LSB.

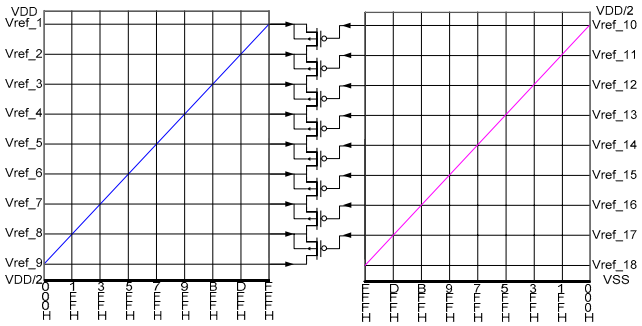

Fig 4. Relations between Vref_1~Vref_9 and Vref_10 ~Vref_18 for constant Vgs

128 to 16 decoder of Fig. 1 forces voltage to gate reference of 8 Active resistor units. Active resistor totally needs 16 gate references, because each active resistor unit needs 2 gate references. In Fig. 4, Vref_1-Vref_10 = Vref_2-Vref_11 = Vref_3-Vref_12 = Vref_4-Vref_13 = …=Vref_9-vref_18 is known, so if Vref_1 and Vref_2 are selected to 3 bit gamma voltage reference decoder, 16 of voltage levels between Vref_10 and Vref_11 become connected to 16 gates of Active resistor unit. According to this method, comparatively same Vgs can be forced to Active resistor. It is necessary for regular Rds.

3. Measurement results

Figure 5 shows the result that we measured real output voltage of 10 bit Active resistor DAC. 10 bit Active resistor DAC was made in 0.35μ m, 16V process, and VDD was measured under the condition of 15V. Fig. 6 shows INL(Integral nonlinearity) of 10 bit Active resistor DAC.[1] The max of INL is -1.5 LSB, and it is not acceptable. DNL(Differential nonlinearity) in Figure 7 is not also acceptable, because the max value is -2 LSB.[1] INL graph in Figure 6 shows that in every 7 bit data, approximately 1.5 LSB of error is taken place. 1.5 LSB is about 10mV, because VDD is equal to 15V, and in case of 10bit, 1 LSB is equal to 7mV.

The reason of this problem is 3 bit gamma reference decoder and Active resistor unit in Fig. 1. 3 bit gamma reference decoder has bulk switch that prevents reverse bias between source and bulk, otherwise active resistor unit has no bulk switch. For instance, in the case where Vref_1 and Vref_2 were selected, the highest voltage is forced to the anode and bulk of Active resistor unit, then reverse bias is not occurred as well as body effect. However when Vref_2 and Vref_3 are selected, lower voltage than cathode would be forced to anode and bulk of active resistor unit. In this case, maximum 32 mV of reverse bias occurs between the source and bulk of PMOS, otherwise there is no avalanche. However, body effect occurs to PMOS used in Active resistor unit, so Vth is increased, and Rds is also increased rather than the PMOS used in 3 bit gamma voltage reference decoder. That is, when Vref_2, Vref_4, Vref_6 and Vref_8 are forced as the highest voltage in cathode of Active resistor unit, body effect occurs and -10mV of output voltage error also occurs because of increasing Rds.

As shown in Fig. 6 and 7, we can reproduce the output voltage error from simulation results. For this reason, we are absolutely sure to solve the problem with the bulk switch of Active resistor unit. If it is not for 1.5 LSB error, INL and DNL of active resistor string DAC are ±0.5 LSB and ±0.3 LSB each other, and both are acceptable.

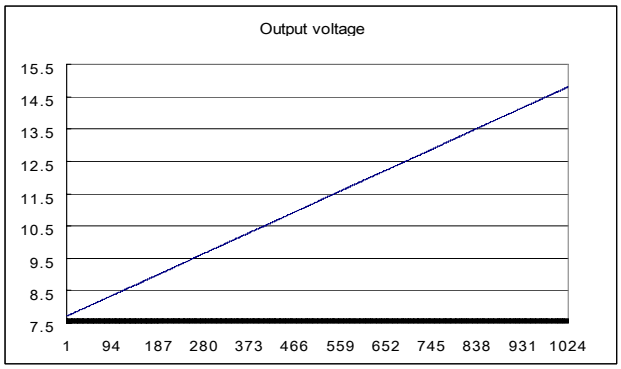

Fig 5. Output voltage measurement result of 10bit linear active resistor string DAC

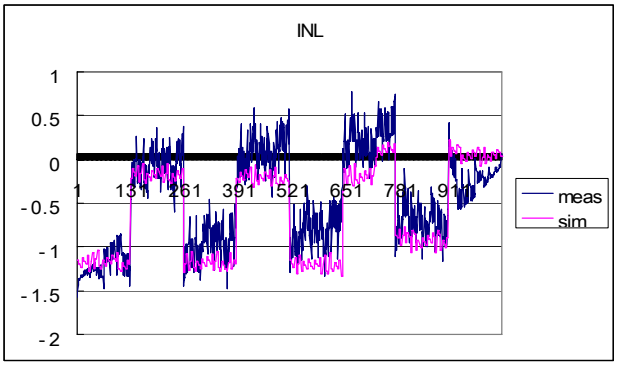

Fig 6. INL of 10bit linear active resistor string DAC

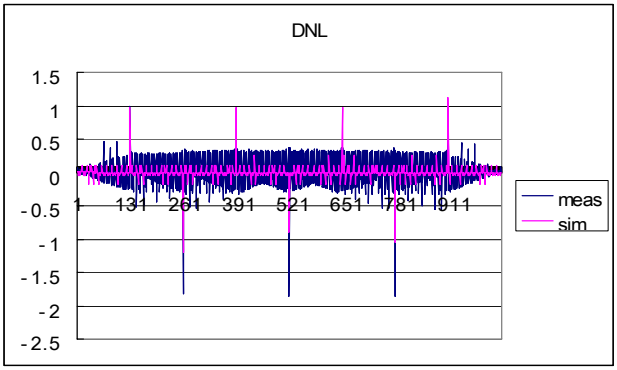

Fig 7. DNL of 10bit linear active resistor string DAC

	A linear active resistor string DAC with an interpolating buffer AMP
Process	0.35μ m CMOS
Operating voltage	15.0 V(analog), 3.0V(logic)
INL	± 0.5 LSB
DNL	± 0.3 LSB
Resolution	10bit

Table 1. Implementation condition & Performance summary

4. Conclusion

As LCD TVs are tending bigger and to implement high quality, TFT LCD source driver IC requires multi gamma function, 10 bit resolution and high speed operation as well as small size. However, existing TFT LCD Source driver IC structure has the limits for satisfaction these all needs.

Table 2 shows a comparison results with each type of DAC. To implementation multi gamma function 12bit linear DAC is essential. So, I estimated 12bit linear passive resistor string DAC and after this, I compared 12bit linear active resistor string DAC with 12bit linear passive resistor string DAC. In this table, 12 bit linear active resistor DAC is more advantageous in RC delay than others. And it is more size efficiency than 12bit linear passive resistor string DAC. It's INL and DNL are inferior in strength than passive resistor string DAC, but it is acceptable.

In this paper, we suggested linear active resistor DAC so that we could solve these problem. Of course Active resistor string DAC can not be a perfect solution for all of the problems. It has the problems, one is output voltage error due to the bulk switch of active resistor unit, and the other is that size is not so efficiency because of the wide gab between wells according to the well to well rule in process. However, the advantages of active resistor string DAC absolutely correspond with the direction which TFT LCD source drive IC should pursue to from now on. We thought that active resistor string DAC would be the applicable and adequate solution for the mentioned problems.

	10bit non linear passive resistor string DAC	12bit linear passive resistor string DAC	12bit linear active resistor string DAC
Decoder stage	8 stage	10 stage	7 stage
INL	± 0.3 LSB	± 0.3 LSB	± 0.5 LSB
DNL	± 0.2 LSB	± 0.2 LSB	± 0.3 LSB
Size	1	4 times	2 times
Multi gamma	Not support	Support	Support
	0.35μ m process, 15.0 V operating voltage, With an interpolating buffer AMP		

Table 2. Comparison results with each type of DAC

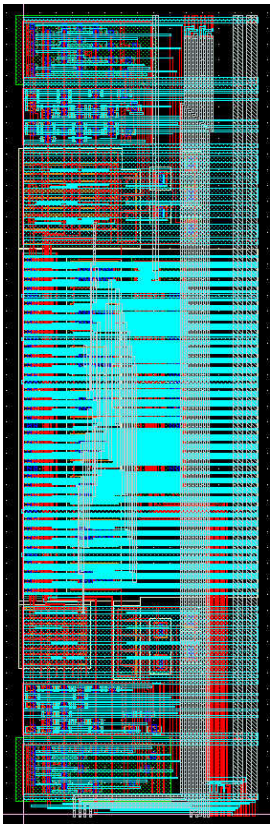

Fig 8. Layout of active resistor string DAC

5. References

[1] Behzad Razavi, "Principles of Data conversion system design",p.45 ,IEEE press, New York(1995)

[2] Po-Ming Lee, Hung-Yi Chen, "Circuits and Systems", 2005. ISCAS 2005. IEEE International Symposium on 23-26 May 2005 Page(s):780 - 783 Vol. 1